Design and Implementation of Low Power Array Multiplier using SERF Full Adder

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Abstract— Power dissipation is the main concerning area in day to day life. Multipliers are the main sources of power dissipation are DSP blocks. In this project design and implementation of the effective low power multipliers with the use of full adders are given. So firstly, we design and simulate the full adders to get the most effective full adders. 1 bit full adder using different xor-xnor gates are designed and analyzed and the analysis is based on simulation parameters like number of transistors, power, delay, power delay product. Each of these circuits cell exhibits different power consumption, delay and area in different VLSI technology. The adders considered are conventional full adder, SERF adder, 13A adder, CLRCL adder, 8T adder. After performing simulation, adder will be chosen according to the performance parameters to design the array multiplier. The SERF full adder has the lowest power consumption. The array multiplier is designed with the help of SERF adder and comparing the result with the normal array multiplier. After calculating the power consumption we have the value for normal and SERF based array multiplier are -1.3E-04 W and -7.7E-04 W respectively. The designs are implemented and power dissipation results are obtained using Cadence Virtuoso tool in 180nm technology.

Index Terms— Array Multiplier. SERF Full Adder, Power Dissipation, Static Energy

1. INTRODUCTION

Low power is the interesting field of electronics which uses less electric power. There are several factors which are responsible for the improvement in performance of the circuits from which power minimization is one of the primary concerns. This factor has the greatest effect on modern VLSI design due to two reasons , one is the long battery operating life requirement and second is due to increasing number of transistors on a single chip leads to a high power dissipation. There are several causes for power consumption out of which important are outnumbered.

1) Dynamic power consumption which is caused by adiabatic charging and discharging of (usually parasitic) capacitances.
2) Static power consumption which corresponds to the non-zero current of transistor in OFF- state.
3) Short Circuit power consumption caused by crow bar flowing through the lapse of time when both PMOS and NMOS transistors are in the ON-state.

So to reduce the load capacitances we have to reduce the total number of parasitic capacitance in internal node. To save the dynamic power consumption by lowering the switching activity.

There are three major sources of power consumption in digital CMOS circuits which are summarized in the equation given below:

$P_{total} = \alpha C_l VDD^2 f_{clk} + I_{sc} VDD + I_{leakage}.VDD$

The first term represents the switching component of power, where α is the switching factor, C_l is the load capacitance, f_{clk} is the clock frequency. In most cases, the voltage swing is the same as the supply voltage VDD, however in some logic circuits, such as in single-gate pass transistor implementations, the voltage swing on some internal nodes may be slightly less. The second term is due to direct path short circuit current I, which arises when both nMOS and pMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current I, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations. The dominant term in a well-designed circuit is the switching component, and low power design thus becomes the task of minimizing C_l, VDD, and f_{clk}, while retaining the required functionality.

The power-delay product can be interpreted as the amount of energy expended in each switching event (or transition) and is thus particularly useful in comparing the power consumption of various circuit styles. If it is assumed that only the switching component of the power consumption is important, then it is given by following equation:

Energy per transition = $P_{total} / f_{clk} = C_l VDD^2$

Where C_l is the load capacitance being switched to perform the computation.

A multiplier is an electronic circuit which is used to multiply two binary numbers. Multipliers are used in a wide range of devices, from large scale processors to small embedded DSP chips. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involved computing a set of partial products and then summing the partial products together. Multipliers are large, slow and complex components. So to make these multipliers effective many steps are taken. Basically multipliers are designed by the help of adders. If adders are power efficient, then only we can design the high speed, low power dissipated multiplier.

We have several types of full adders i.e. SERF full adder, CLRCL full adder, 13A full adder, 8T full adder, 6T full adder which are known as their own effective performance parameter. Conventional 28T full adder is best known for less delay but we cannot use this full adder due to more power dissipation and large area. So here we used the SERF adder which consumes less power dissipation than others. The key to use less power is the reuse of charge which is drained during logic low. Charged is used as input signal to control the gates of transistor. As there is no direct path to ground, the power dissipation due to short circuit current is completely reduced. Here the full adder is design by using pass transistor logic xor-xnor gates.

2. SERF ADDER

SERF is a 10 transistor full adder. We have the following equations for SUM and COUT.

$Sum = (A\overline{\oplus}B)Cin + (A\oplus B)\overline{Cin}$

$Cout = (A\oplus B)Cin + (A\overline{\oplus}B)A$

This transistor is far better than the 28T full adder. Firstly, it consist of 28 transistors. Using of 28 transistors allowing the increment of power dissipation than 10 transistors full adders. 28T full adder is only good for delay factor not for power dissipation. The beauty of SERF full adder is to recovery of charge current. The charge which is drained during logic low is reused. It is use as a input signal to control the gates of transistor. As there is no direct path to ground, hence the power dissipation due to short circuit current is completely reduced. By this way static energy is recovered. This circuit well operates at higher supply voltages, but if the supply voltage scaled to voltage lower than 0.3V, this circuit will fail to work. Table 1 shows the SERF operation with different input signals. As it can be seen the SERF adder is confronted with serious problems especially at lower supply voltage. Assume that one of the two input vectors ABC_{in} = "110" and "111" are applied. Now if C_{in} =0 then C_{out} will be equal to V_{dd}-2V_{th} and Sum signal is going to zero driven by MOS transistor with its gate connected to V_{dd}-V_{th}. When C_{in}=1, C_{out} is connected to V_{dd} (may be lower) and the SUM signal will go to V_{dd}- V_{th}. Another problem with this design is when the floating node is connected to 0 (A=0, B=1 or A=1, B=0).When C_{in} is "1", C_{out} is charged to V_{dd}, but when C_{in}=0, C_{out} must be discharged to ground using a PMOS pass transistor that cannot fully discharge the output. In this case, C_{out} is discharged to V_{tp} which is higher than V_{tn}. This problem is intensified if the circuit works at sub threshold voltage.

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	Vdd-Vth	~=0
0	1	0	1	Vtp
0	1	1	0	1
1	0	0	1	>Vtp
1	0	1	0	1
1	1	0	POWER CON-SUMING	Vdd-2Vth
1	1	1	>Vdd-2Vth	Vdd-Vth

TABLE 1: TRUTH TABLE OF SERF FULL ADDDER

The most vital issue with SERF full adder is for the situation when A=1, B=1 and Cin=0. For this situation as specified before the output signal achieves Vdd. Simulation results demonstrate that at Vdd=0.3V, the output signal is rising just to 0.1V which is not sufficiently high to change the state of the next stage. To take out these issues another topology must be presented. This impediment likewise causes a requirement for bringing down the supply voltage. Case in point, to have a right output for SUM it appears that the supply voltage can't be brought down more than Vdd/2+2Vtn demonstrating that the supply voltage must be higher than Vdd/2+0.28V in a 65nm CMOS technology. Notwithstanding this farthest point relies on upon the circuit design topology furthermore the measuring and the device sorts that are utilized. To relieve this issue, the gates of pass transistors for Cout signal must be associated with Vdd during the testing state (A=B=1, Cin=0). At that point the supply voltage might be diminished to as low as Vdd/2+Vth which is evaluated to be Vdd/2+0.14. For instance when Vdd=0.3, in most worst case Cout will then be Vdd-Vth=0.16V, which can be utilized as a high logic. Also the NMOS pass transistor might be upsized to further lower the supply voltage. It is by all accounts conceivable to lower supply voltage to 0.25V. In A=1, B=1, and Cin=0, the identical circuit for SUM sign is appeared in Figure 2. As it can be seen, we can't choose precisely the condition of the output, on the grounds that, for this situation, two PMOS gadgets furthermore the NMOS transistors are ON, then the output state is generally dependant on the transistor. As a result the circuit neglects to assess accurately now and again.

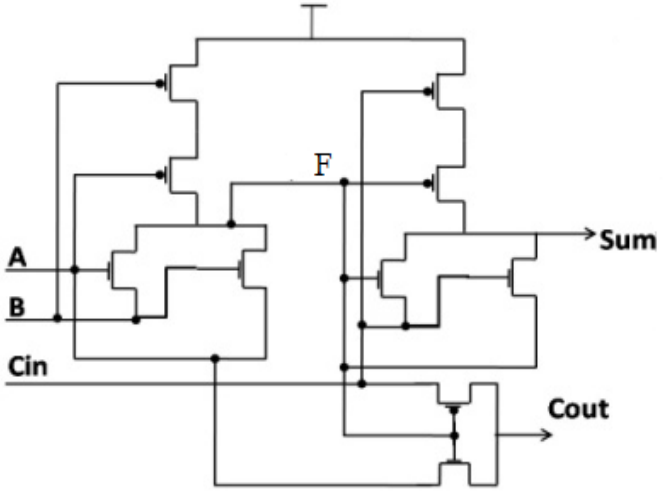

Fig 1: SERF adder

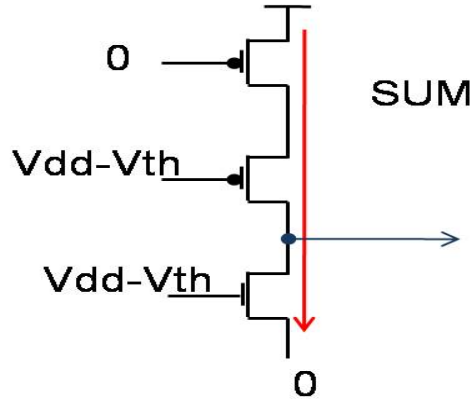

Fig 2: Equivalent circuit in input vector ABCin = "110"

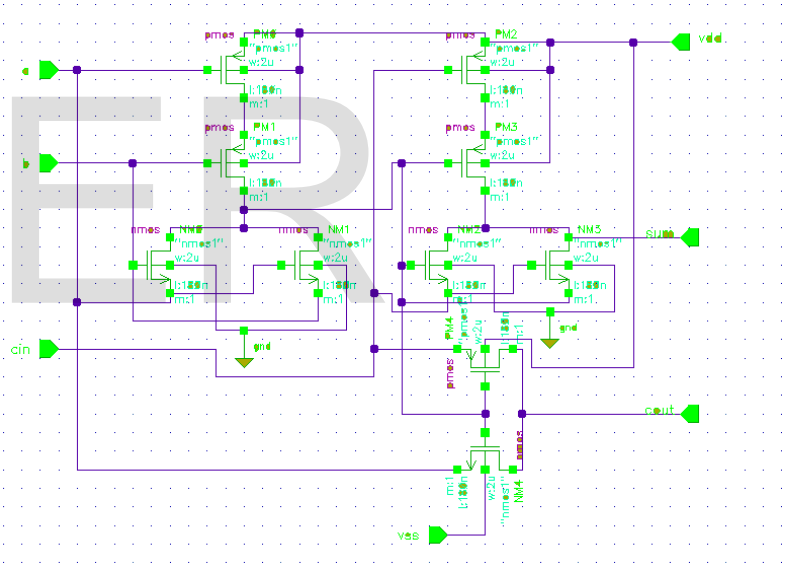

Fig 3: Schematic of SERF Full Adder

3 ARRAY MULTIPLIER

Array multiplier is well known as due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of multiplicand with one multiplier bit. The partial products are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adders. N-1 adders are required where N is the multiplier length.

			X3	X2	X1	X0	
		x	Y3	Y2	Y1	Y0	
			Y0	x Y0 x	Y0 x	Y0 x	
		C	X3	X2	X1	X0	
		Y1 x	Y1 x	Y1 x	Y1 x		
	+	X3	X2	X1	X0		
	C	sum	sum	sum	sum		
	Y2 x	Y2 x	Y2 x	Y2 x			
+	X3	X2	X1	X0			
C	sum	sum	sum	sum			
Y3 x	Y3 x	Y3 x	Y3 x				
+ X3	X2	X1	X0				
C sum	sum	sum	sum				
P7	P6	P5	P4	P3	P2	P1	P0

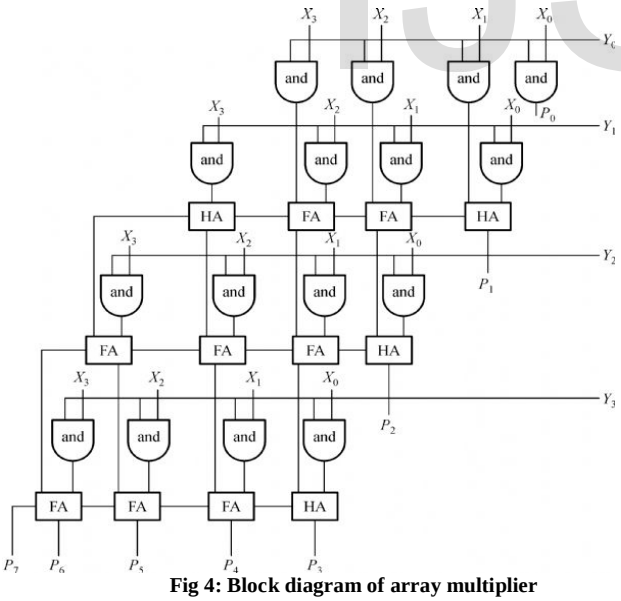

Fig 4: Block diagram of array multiplier

In array multiplication we have to add the same numbers of partial products as there are multiplier bits. In order to perform signed multiplication, 2's complement number system is used to represent the multiplicand and the multiplier. This suggests every one of the adders in a specific stage ought to be of equal bit length. To accomplish this, the sign bits of the partial products in the initial row and the sum and carry signs of every adder stage are augmented. The augmentation is completed until the signs width matches the width of the largest absolute value signal in that stage. Additionally, the generation of X partial products requires X×Y two-bit AND gates. Large area of the multiplier is committed to perform addition of N partial products, which require (N −1) M-bit adders. The shifting of the partial products for appropriate arrangement is performed by simple routing and does not require any logic. The array structure makes it a troublesome errand to quantify the propagation delay. There are more than one identical length basic timing ways accessible in the circuit.

4. PROPOSED DESIGN

The 4*4 array multiplier using SERF FUL ADDER is our proposed design. It consist of sixteen 2-bit AND gates, four 2-bit half adder and eight 3-bit SERF full adder. AND gate consists of one NAND gate and an inverter. Half adder consistS of one XOR gate and an inverter. Fig 5 is our proposed schematic of array multiplier using SERF full adder.

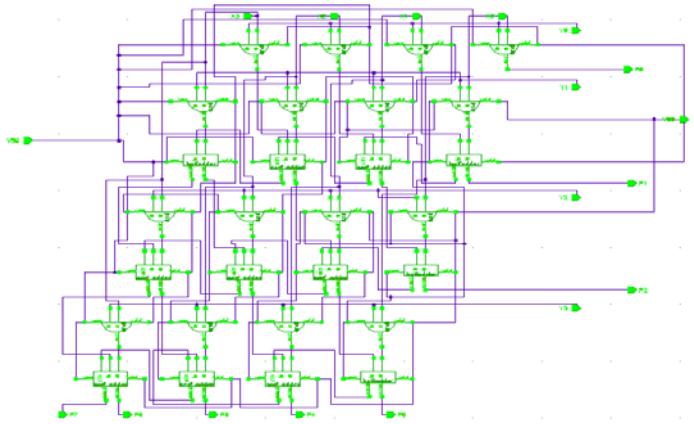

Fig 5: Schematic shows array multiplier using SERF adder

5. SIMULATIONS AND COMPARISONS

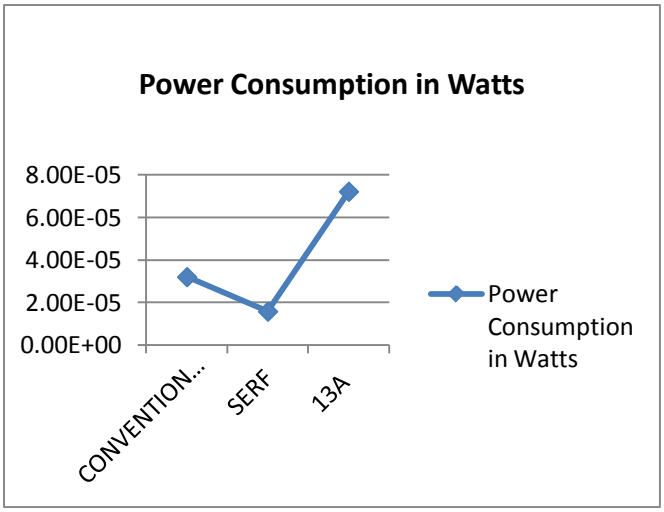

Fig 8: Graph shown the power consumption for Full Adders

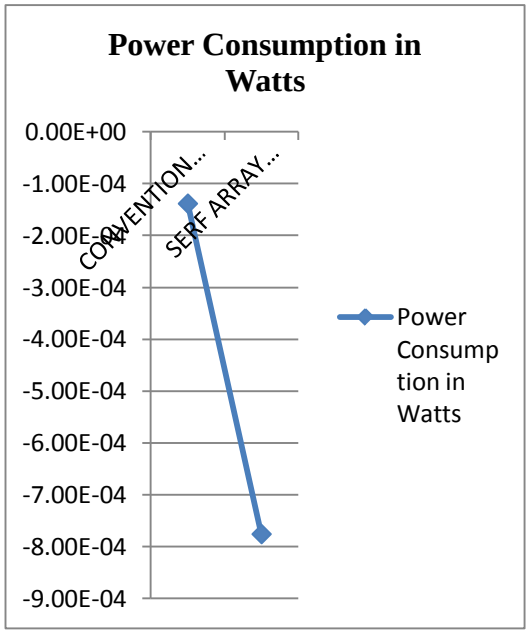

Fig 9: Graph shown the power consumption of Array Multiplier

TYPES OF FULL ADDERS	POWER CONSUMPTION(FOR 5V)
CONVENTIONAL FULL ADDER	32.04E-06 W
SERF FULL ADDER	15.79E-06 W

Table 2

TYPES OF MULTIPLIERS	POWER CONSUMPTION(FOR 3.3V)
ARRAY MULTIPLIER	-1.3E-04 W
SERF ARRAY MULTIPLIER	-7.7E-04 W

Table 3

The pre-layout simulations are done at 180nm technology. Graphs shown in fig 8 and fig 9 depicts that the proposed 4*4 array multiplier is the viable option for efficient design. The graph shown in fig 9 reveals that the power consumption of the proposed 4*4 array multiplier is remarkably less than the conventional array multiplier.

6. CONCLUSION

We have successfully simulated the various full adders and after calculating the power consumption we come to know that the SERF adder is best known for the designing of low power multipliers. By the help of this specific low power adder we designed the array multiplier. Beside of this array multiplier we designed the conventional array multiplier to compare the results of these two. Our requirement was to get the lowest power array multiplier, so we get it after compare the results.

7. REFERENCE

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